Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request;[[,]]

identifying a data element in the allocation register having a value corresponding to an available buffer,[[;]]

changing the value of said data element to a value corresponding to an allocated buffer,[[;]] and

allocating the buffer associated with said data element;

monitoring the values of each of the data elements in the allocation register; and

in response to each of the data elements having the value corresponding to an allocated buffer:

writing the data elements in the allocation register back to the allocation memory,

identifying a set including at least one data element having the value corresponding to an available buffer, and

writing the set to the allocation register.

2. (Original) The method of claim 1, wherein each of the plurality of data elements comprises a single bit.

3. (Original) The method of claim 1, wherein each of the plurality of sets comprises a line in the allocation memory.

4. (Original) The method of claim 1, further comprising:

in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and

changing a value of said data element to the value corresponding to an available buffer.

5. (Original) The method of claim 4, further comprising:

in response to identifying the data element associated with said buffer in the allocation memory,

writing the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

writing the set in the clear register to the allocation memory.

6. (Canceled)

7. (Currently amended) The method of claim 1 [[6]], further comprising:

providing a vector including a plurality of data elements, [[,]]each data element being associated with a corresponding one of the plurality of sets;

changing a value of a data element in the vector from the allocation register to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory; and

changing the value of said data element in the vector to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

8. (Original) The method of claim 7, further comprising:

identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

9-17. (Canceled)

18. (Currently amended) An apparatus comprising:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager to:

write one of said plurality of sets into the allocation register~~;~~ ~~and~~

in response to an allocation request;[[,]]

identify a data element in the allocation register having a value corresponding to an available buffer,

change the value of said data element to a value corresponding to an allocated buffer, and

allocate the buffer associated with said data element;

monitor the values of each of the data elements in the allocation register; and

in response to each of the data elements having the value corresponding to an allocated buffer:

write the data elements in the allocation register back to the allocation memory,

identify a set including at least one data element having the value corresponding to an available buffer, and

write the set to the allocation register.

19. (Original) The apparatus of claim 18, wherein each of the plurality of data elements comprises a single bit.

20. (Original) The apparatus of claim 18, wherein each of the plurality of sets comprises a line in the allocation memory.

21. (Original) The apparatus of claim 18, wherein the buffer manager is further operative to:

in response to a clear request for one of the plurality of buffers,

identify a data element associated with said buffer in one of the allocation memory and the allocation register; and

change a value of said data element to the value corresponding to an available buffer.

22. (Original) The apparatus of claim 21, wherein the buffer manager is further operative to:

in response to identifying the data element associated with said buffer in the allocation memory,

write the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

write the set in the clear register to the allocation memory.

23. (Canceled)

24. (Currently amended) The apparatus of claim 18 [[23]], further comprising:

a line indication module to

generate a vector including a plurality of data elements, each data [[.]]element being associated with a corresponding one of the plurality of sets,

change a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data[[,]] element in the vector to the allocation memory, and

change the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

25. (Original) The apparatus of claim 24, wherein the line indication module is further operative to:

identify a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

26. (Original) The apparatus of claim 18, wherein the allocation memory comprises an SRAM.

27-55. (Canceled)

56. (Currently amended) A system comprising:

a switching module to receive and switch packets;

a buffer memory including a plurality of buffers to store received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding one of the plurality of buffers in the buffer memory;

an allocation register; and

a buffer manager to:

write one of said plurality of sets into the allocation register~~;~~ ~~and~~

in response to an allocation request;[[,]]

identify a data element in the allocation register having a value corresponding to an available buffer,

change the value of said data element to a value corresponding to an allocated buffer, and

allocate the buffer associated with said data element;

monitor the values of each of the data elements in the allocation register; and

in response to each of the data elements having the value corresponding to an allocated buffer:

write the data elements in the allocation register back to the allocation memory,

identify a set including at least one data element having the value corresponding to an available buffer, and

write the set to the allocation register.

57. (Original) The system of claim 56, wherein each of the plurality of data elements comprises a single bit.

58. (Original) The system of claim 56, wherein each of the plurality of sets comprises a line in the allocation memory.

59. (Original) The system of claim 56, wherein the buffer manager is further operative to:

in response to a clear request for one of the plurality of buffers,

identify a data element associated with said buffer in one of the allocation memory and the allocation register; and

change a value of said data element to the value corresponding to an available buffer.

60. (Original) The system of claim 59, wherein the buffer manager is further operative to:

in response to identifying the data element associated with said buffer in the allocation memory,

write the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

write the set in the clear register to the allocation memory.

61. (Canceled)

62. (Currently amended) The system of claim 56 [[61]], further comprising:

a line indication module to

generate a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets,

change a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory, and

change the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

63. (Original) The system of claim 62, wherein the line indication module is further operative to:

identify a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

64. (Original) The system of claim 56, wherein the allocation memory comprises, an SRAM.

65-74. (Canceled)

75. (Currently amended) A system comprising:

a switching module including means for receiving and switching packets;

a buffer memory including a plurality of buffers for storing received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager including:

means for writing one of said plurality of sets into the allocation register~~;~~ ~~and~~

means for, in response to an allocation request;[[,]]

identifying a data element in the allocation register having a value corresponding to an available buffer,

changing the value of said data element to a value corresponding to an allocated buffer, and

allocating the buffer associated with said data element;

means for monitoring the values of each of the data elements in the allocation register;

means for, in response to each of said data elements having the value corresponding to an allocated buffer;

writing the data elements in the allocation register back to the allocation memory,

identifying a set including at least one data element having the value corresponding to an available buffer, and

writing the set to the allocation register.

76. (Original) The system of claim 75, wherein each of the plurality of data elements comprises a single bit.

77. (Original) The system of claim 75, wherein each of the plurality of sets comprises a line in the allocation memory.

78. (Original) The system of claim 75, wherein the buffer manager further comprises:

means for, in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register, and

changing a value of said data element to the value corresponding to an available buffer.

79. (Original) The system of claim 78, wherein the buffer manager further comprises:

means for writing the set including said data element to a clear register in response to identifying the data element associated with said buffer in the allocation memory; and

means for writing the set in the clear register to the allocation memory after changing the value of said data element in the clear register.

80. (Canceled)

81. (Currently amended) The system of claim 75 [[80]], further comprising:

means for generating a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets;

means for changing a value of a data element in the vector to a value corresponding to a

full set in response to writing the set associated with said data element in the vector to the allocation memory; and

means for changing the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of [[,]]one of the data elements in said set being changed to the value corresponding to an available buffer.

82. (Original) The system of claim 81, further comprising:

means for identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

83. (Original) The system of claim 75, wherein the allocation memory comprises an SRAM.

84-93. (Canceled)

94. (Currently amended) A computer-readable medium having instructions stored thereon, which, when executed by a processor, causes the processor to perform operations comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request;[[,]]

identifying a data element in the allocation register having a value corresponding to an available buffer;[[;]]

changing the value of said data element to a value corresponding to an allocated buffer;[[;]] and

allocating the buffer associated with said data element;

monitoring the values of each of the data elements in the allocation register; and

in response to each of the data elements having the value corresponding to an allocated buffer:

writing the data elements in the allocation register back to the allocation memory,

identifying a set including at least one data element having the value corresponding to an available buffer, and

writing the set to the allocation register.

95. (Previously presented) The computer-readable medium of claim 94, wherein each of the plurality of data elements comprises a single bit.

96. (Previously presented) The computer-readable medium of claim 94, wherein each of the plurality of sets comprises a line in the allocation memory.

97. (Previously presented) The computer-readable medium of claim 94, further comprising:

in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and

changing a value of said data element to the value corresponding to an available buffer.

98. (Previously presented) The computer-readable medium of claim 97, further comprising:

in response to identifying the data element associated with said buffer in the allocation memory,

writing the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

writing the set in the clear register to the allocation memory.

99. (Canceled)

100. (Currently amended) The computer-readable medium of claim 94 [[99]], further comprising:

providing a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets;

changing a value of a data element in the vector from the allocation register to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory; and

changing the value of said data element in the vector to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

101. (Previously presented) The computer-readable medium of claim 100, further comprising:

identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

102-110. (Canceled)

111. (Previously presented) The method of claim 1, wherein each of the plurality of sets is a non-empty set.

112. (New) A method comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of the data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request:

identifying a data element in the allocation register having a value corresponding to an available buffer,

changing the value of the data element to a value corresponding to an allocated buffer, and

allocating the buffer associated with the data element; and

in response to a clear request for one of the plurality of buffers:

identifying a data element associated with the buffer in one of the allocation memory and the allocation register, and

changing a value of the data element to a value corresponding to an available buffer,

in response to identifying the data element associated with said buffer in the allocation memory:

writing the set including said data element to a clear register, and

after changing the value of said data element in the clear register, writing the set in the clear register to the allocation memory.

113. (New) An apparatus comprising:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of the data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager to:

write one of the plurality of sets into the allocation register;

in response to an allocation request:

identify a data element in the allocation register having a value corresponding to an available buffer,

change the value of the data element to a value corresponding to an allocated buffer, and

allocate the buffer associated with the data element;

in response to a clear request for one of the plurality of buffers:

identify a data element associated with the buffer in one of the allocation memory and the allocation register, and

change a value of the data element to a value corresponding to an available buffer; and

in response to identifying the data element associated with the buffer in the allocation memory:

write the set including the data element to a clear register, and

after changing the value of the data element in the clear register, write the

set in the clear register to the allocation memory.

114. (New) A system comprising:

a switching module to receive and switch packets;

a buffer memory including a plurality of buffers to store received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of the data elements being associated with a corresponding one of the plurality of buffers in the buffer memory;

an allocation register; and

a buffer manager to:

write one of the plurality of sets into the allocation register;

in response to an allocation request:

identify a data element in the allocation register having a value corresponding to an available buffer,

change the value of the data element to a value corresponding to an allocated buffer, and

allocate the buffer associated with the data element;

in response to a clear request for one of the plurality of buffers:

identify a data element associated with the buffer in one of the allocation memory and the allocation register, and

change a value of the data element to a value corresponding to an available buffer, and

in response to identifying the data element associated with the buffer in the allocation memory:

write the set including the data element to a clear register, and

after changing the value of the data element in the clear register, write the set in the clear register to the allocation memory.

115. (New) A system comprising:

a switching module including means for receiving and switching packets;

a buffer memory including a plurality of buffers for storing received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of the data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager including:

means for writing one of the plurality of sets into the allocation register;

mans for, in response to an allocation request:

identifying a data element in the allocation register having a value corresponding to an available buffer,

changing the value of the data element to a value corresponding to an allocated buffer,

allocating the buffer associated with the data element;

means for, in response to a clear request for one of the plurality of buffers:

identifying a data element associated with the buffer in one of the allocation memory and the allocation register; and

changing a value of the data element to a value corresponding to an available buffer;

means for writing the set including the data element to a clear register in response to identifying the data element associated with the buffer in the allocation memory; and

means for writing the set in the clear register to the allocation memory after changing the value of the data element in the clear register.

116. (New) A computer-readable medium having instructions stored thereon, which, when executed by a processor, causes the processor to perform operations comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of the data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request:

identifying a data element in the allocation register having a value corresponding to an available buffer,

changing the value of the data element to a value corresponding to an allocated buffer, and

allocating the buffer associated with the data element;

in response to a clear request for one of the plurality of buffers:

identifying a data element associated with the buffer in one of the allocation memory and the allocation register, and

changing a value of the data element to a value corresponding to the available buffer; and

in response to identifying the data element associated with the buffer in the allocation memory:

writing the set including the data element to a clear register, and

after changing the value of the data element in the clear register, writing the set in the clear register to the allocation memory.